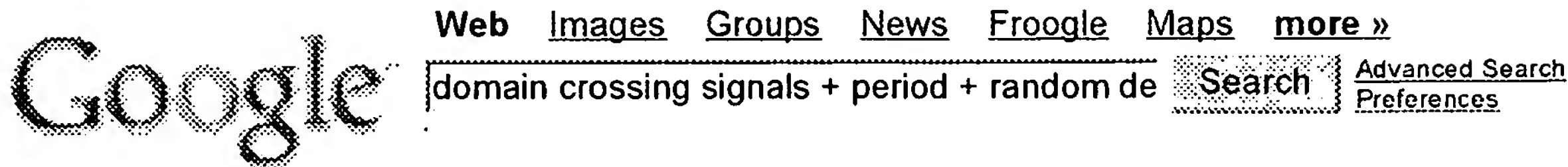


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Web Results 1 - 10 of about 19,600 for domain crossing signals + period + random delay + flip-flop. (0.66 s)

EETimes.com - Clock **domain** modeling is essential in high density ...

All clock **domain crossing** logic should be contained in the bus adapter module. ... naturally introduces a one or two receive clock **period delay**, ...

www.eetimes.com/in_focus/embedded_systems/OEG20030606S0036 - 74k -

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[PDF] Clock **domain** modeling is essential in high density design

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Because the synchronizer imposes a two receive clock **delay** and because at ... **domain crossing** of the pointers and read/write **signals**. ...

www.fulcrummicro.com/tech_resources/eetimes_03-0606_03.pdf - [Similar pages](#)

Semiconductor device for **domain crossing** - Patent 6980479

a **domain crossing** sensing block in response to a operation mode **signal**, first and second **delay locked loop (DLL) clock signals** and a CAS latency for ...

www.freepatentsonline.com/6980479.html - 73k - [Cached](#) - [Similar pages](#)

[PDF] A 0.7–2-GHz Self-Calibrated Multiphase **Delay-Locked Loop**

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clock **period**. Assume that. is the **delay** time of the ith. **delay cell**, ... PD, implemented by a current-mode-logic D-**flip-flop** (CML ...

ieeexplore.ieee.org/iel5/4/34101/01624394.pdf?tp=a&arnumber=1624394 - [Similar pages](#)

FPGA-FAQ 0017 Tell me about Metastability

Since all flops are clocked by the same clock **signal**, all logic paths have the same worstcase **delay** requirements, which is clock **period** minus **flipflop** ...

www.fpga-faq.com/FAQ_Pages/0017_Tell_me_about_metastables.htm - 46k -

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FPGA FAQ comp.arch.fpga archives - messages from 29675

De-rate > the Tco of the **domain crossing** FFs by some multiple, say 6, of the unrouted > **delay**. Then set up constraints like this: > > TIMESPEC TSSync = FROM ...

www.fpga-faq.com/archives/29675.html - 74k - [Cached](#) - [Similar pages](#)

Clock **domain** modeling is essential in high density SoC design

Applying synchronizers is further complicated by **domain crossing** vectors where all bits of ... naturally introduces a one or two receive clock **period delay**, ...

www.us.design-reuse.com/news/?id=5678&print=yes - 30k - [Cached](#) - [Similar pages](#)

Using **delay** - Patent Storm

A method for distributing clocks to **flip-flop** circuits which constitute a logic ... The **signal** phase shifting circuit includes a reference **signal period** ...

www.patentstorm.us/class/713/401-Using_delay.html - 47k - [Cached](#) - [Similar pages](#)

[PDF] Chapter 12. DE **Domain**

File Format: PDF/Adobe Acrobat - [View as HTML](#)

Flip Flop p. T. Clk. Q. Q'. Specific to the DE **Domain** ... counting process) through two channels with **random delay**, and. merge the channel outputs. sampler ...

ptolemy.eecs.berkeley.edu/ptolemyclassic/almagest/docs/user/pdf/de.pdf - [Similar pages](#)